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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,403	01/26/2004	Ho-young Song	5649-1180	2218
20792	7590	08/09/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC			CHO, JAMES HYONCHOL	
PO BOX 37428			ART UNIT	
RALEIGH, NC 27627			PAPER NUMBER	
			2819	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/765,403	<b>Applicant(s)</b> SONG, HO-YOUNG	
	<b>Examiner</b> James Cho	<b>Art Unit</b> 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-19 is/are allowed.
- 6) ☒ Claim(s) 20-43 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

Figure 5A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 20-43 are rejected under 35 U.S.C. 102(b) as being anticipated by Coteus et al. (US PAT No. 6,127,840).

Regarding claim 20, Fig. 2 of Coteus et al. discloses a termination circuit which reduces ringing and dynamic current, which occur when an input signal (signal at node 30) is transmitted through a transmission line (94), the termination circuit comprising: a first switching unit (36,38) which includes a first termination resistor (38) used to form a path for current flow (current flow from node 30 to VSS) between a first node (30) and a

Art Unit: 2819

first voltage (VSS) when a voltage level of the input signal is inverted to a first level (signal at node 30 changing from logic high to logic low) ; and a second switching unit (32,34) which includes a second termination resistor (34) used to form a path for current flow (current flow from node 30 to VSS) between the first node and a second voltage (VSS) when the voltage level of the input signal is inverted to a second level (signal at node 30 changing from logic low to logic high), wherein termination resistance of the first and second switching units are maintained level to a resistance of the transmission line when the voltage level of the input signal is inverted (col. 3, lines 45-50).

Regarding claim 21, Fig. 2 of Coteus et al. discloses the termination circuit of claim 20 where the first switching unit comprises a first transistor (36), including a first end connected to the first voltage (36 coupled to VSS) and a gate receiving the input signal (gate of 36 receives the input signal via 42), and the first termination resistor (38) which is connected between a second end of the first transistor and the first node (38 coupled between the node 30 and 36).

Regarding claim 22, Fig. 2 of Coteus et al. discloses the termination circuit of claim 21 where the first switching unit further comprises a first resistor (82 in Fig. 3A) which is used to protect the gate of the first transistor (ESD protection) and positioned between the first node and the gate of the first transistor (between the node coupling 22 and the gate of 36 via 42).

Regarding claim 23, Fig. 2 of Coteus et al. discloses the termination circuit of claim 21 where the first transistor is an NMOS transistor (36 is NMOS).

Regarding claim 24, Fig. 2 of Coteus et al. discloses the termination circuit of claim 20 where the second switching unit comprises a second transistor (32), including a first end connected to the second voltage (32 coupled to VDD) and a gate receiving the input signal (gate of 32 receives the input signal via 40), and the second termination resistor (34) which is connected between a second end of the second transistor and the first node (34 coupled between the node 30 and 32).

Regarding claim 25, Fig. 2 of Coteus et al. discloses the termination circuit of claim 24 wherein the second switching unit further comprises a second resistor (82 in Fig. 3A) which is used to protect the gate of the second transistor (ESD protection) and is positioned between the first node and the gate of the second transistor (82 coupled between the node coupling 22 and the gate of 32 via 40).

Regarding claim 26, Fig. 2 of Coteus et al. discloses the termination circuit of claim 25 wherein the second transistor is a PMOS transistor (32 is PMOS).

Regarding claim 27, Fig. 2 of Coteus et al. discloses the termination circuit of claim 20 wherein a voltage level of the first voltage is the same as a voltage level of a ground voltage (logic low voltage at 30 enables termination of 36), and a voltage level of

Art Unit: 2819

the second voltage is the same as a voltage level of a supply voltage (logic high voltage at 30 enables 32).

Regarding claim 28, Fig. 2 of Coteus et al. discloses the termination circuit of claim 20 wherein the first level is high and the second level is low (In claim 20, the first switching unit can be 32 and 34 and the second switching unit being 36 and 38. or vice versa for the purpose of name designations where the logic applied to 30 enables 32 and logic low applied to 30 enables 36).

Regarding claim 29, Fig. 2 of Coteus et al. discloses the termination circuit of claim 20, where the termination circuit is mounted in a semiconductor chip (20 is receiving circuit of the second integrated circuit; col. 3, lines 5-10).

Regarding claim 30, Fig. 2 of Coteus et al. discloses a termination circuit (20) which reduces ringing and dynamic current which occurs when an input signal is transmitted through a transmission line (22), the termination circuit comprising: a first termination unit (36,38, 42) which includes a first termination resistor (38) allowing impedance matching to be performed by using a ground voltage (logic low at node 30) when a voltage level of the input signal is inverted to high (logic low at node 30 is inverted to high via 42 and enables 36); and a second termination unit (32,34,40) which includes a second termination resistor (34) allowing impedance matching to be performed by using a supply voltage (logic high at node 30) when a voltage level of the

Art Unit: 2819

input signal is inverted to low (logic high at node 30 inverted to logic low via 40 which enables 32), wherein termination resistance of the first and second termination units are maintained level to a resistance of the transmission line when the voltage level of the input signal is inverted (col. 3, lines 45-50).

Regarding claim 31, Fig. 2 of Coteus et al. discloses the termination circuit of claim 30, wherein the first termination unit further comprises an NMOS transistor (36), including a first end connected to the ground voltage (36 coupled to VSS) and a gate receiving the input signal (gate of 36 receives the input signal via 42), and the first termination resistor (38) which is connected between a second end of the NMOS transistor and the first node (38 coupled between the node 30 and 36).

Regarding claim 32, Fig. 2 of Coteus et al. discloses the termination circuit of claim 31 where the first termination unit further comprises a first resistor (82 in Fig. 3A) which is used to protect the gate of the NMOS transistor (ESD protection) and positioned between the first node and the gate of the NMOS transistor (between the node coupling 22 and the gate of 36 via 42).

Regarding claim 33, Fig. 2 of Coteus et al. discloses the termination circuit of claim 30, where the second termination unit comprises a PMOS transistor (32), including a first end connected to the second voltage (32 coupled to VDD) and a gate receiving the input signal (gate of 32 receives the input signal via 40), and the second

Art Unit: 2819

termination resistor (34) which is connected between a second end of the PMOS transistor and the first node (34 coupled between the node 30 and 32).

Regarding claim 34, Fig. 2 of Coteus et al. discloses the termination circuit of claim 24 wherein the second switching unit further comprises a second resistor (82 in Fig. 3A) which is used to protect the gate of the PMOS transistor (ESD protection) and is positioned between the first node and the gate of the PMOS transistor (82 coupled between the node coupling 22 and the gate of 32 via 40).

Regarding claim 35, Fig. 2 of Coteus et al. discloses the termination circuit of claim 30, where the termination circuit is mounted in a semiconductor chip (20 is receiving circuit of the second integrated circuit; col. 3, lines 5-10).

Regarding claim 36, Fig. 2 of Coteus et al. discloses a termination circuit (20) which reduces ringing and dynamic current which occurs when an input signal is transmitted through a transmission line (22), the termination circuit comprising: a pull-down unit (36,38, 42) which prevents a voltage level at a first node from reaching a voltage level of a second voltage (VDD) when a voltage level of the input signal is inverted to high (logic low at node 30 is inverted to high via 42 and enables 36); and a pull-up unit (32,34,40) which prevents a voltage level at the first node from reaching a voltage level of a first voltage (VSS) when a voltage level of the input signal is inverted to a second level (logic high at node 30 inverted to logic low via 40 which enables 32).

Regarding claim 37, Fig. 2 of Coteus et al. teaches the termination circuit of claim 36, the pull-down unit further comprises: an NMOS transistor (36) including a first end connected to the first voltage (VSS) and a gate receiving the input signal (gate receives signal at node 30 via 42); and a first termination resistor (38) which is connected between a second end of the NMOS transistor and the first node (38 coupled between 30 and 36).

Regarding claim 38, Fig. 2 of Coteus et al. discloses the termination circuit of claim 37 where the pull-down unit further comprises a first resistor (82 in Fig. 3A) which is used to protect the gate of the NMOS transistor (ESD protection) and positioned between the first node and the gate of the NMOS transistor (between the node coupling 22 and the gate of 36 via 42).

Regarding claim 39, Fig. 2 of Coteus et al. discloses the termination circuit of claim 36, where the pull-up unit further comprises a PMOS transistor (32), including a first end connected to the second voltage (32 coupled to VDD) and a gate receiving the input signal (gate of 32 receives the input signal via 40), and the second termination resistor (34) which is connected between a second end of the PMOS transistor and the first node (34 coupled between the node 30 and 32).

Art Unit: 2819

Regarding claim 40, Fig. 2 of Coteus et al. discloses the termination circuit of claim 39 wherein the pull-up unit further comprises a second resistor (82 in Fig. 3A) which is used to protect the gate of the PMOS transistor (ESD protection) and is positioned between the first node and the gate of the PMOS transistor (82 coupled between the node coupling 22 and the gate of 32 via 40).

Regarding claim 41, Fig. 2 of Coteus et al. discloses the termination circuit of claim 36 wherein a voltage level of the first voltage (VSS is a ground) is the same as a voltage level of a ground voltage, and a voltage level of the second voltage (VDD is the supply voltage) is the same as voltage level of a supply voltage.

Regarding claim 42, Fig. 2 of Coteus et al. discloses the termination circuit of claim 36, wherein the first level is high (logic high) and the second level is low (logic low).

Regarding claim 43, Fig. 2 of Coteus et al. discloses the termination circuit of claim 36, wherein the termination circuit is mounted in a semiconductor chip (20 is receiving circuit of the second integrated circuit; col. 3, lines 5-10).

***Allowable Subject Matter***

Claims 1-19 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: Although, Coteus et al. teaches dynamic line termination clamping circuit, one of ordinary skill in the art would not have been motivated to modify the teachings of Coteus et al. to further include, among other things, the specifics of the first reference voltage being less than the second reference voltage, and the first voltage level being greater than the second voltage level as required by claims 1 and 15.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Igarashi et al. (US PAT No. 5,329,190) discloses a termination circuit.

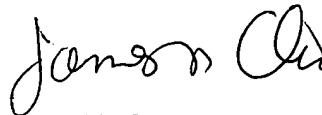
Whitworth (US PAT No. 6,747,476) discloses a method and apparatus for non-linear termination of a transmission line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2819

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "James H. Cho", with a stylized flourish at the end.

James H. Cho  
Primary Examiner  
Art Unit 2819

August 4, 2005